CLOCK STABILIZATION DETECTION FOR HARDWARE SIMULATION

ABSTRACT

Method and apparatus for clock stabilization detection for hardware simulation is described. More particularly, a lock signal is obtained, for example from a digital clock module. A least common multiple (LCM) clock signal is generated, for example from a clock module. A control signal is generated at least partially responsive to the LCM clock signal and the lock signal. The control signal may be generated from a state machine and applied to select circuitry, where the control signal is used to mask application of the output clock signal responsive to the control signal.